	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	168344	e-beam or "electron beam" or ebeam	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:54
2	BRS	L2	289365	SiN or "silicon nitride" or Si?N?	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:54
3	BRS	L3	19113	"self align contact" or SAC or (self-align adj contact)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:55
4	BRS	L4	455538	cathode or anode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:55
5	BRS	L5	55102	(SiH or "NH.sub.3" or "Si.sub.2H.sub.6")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:56

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	3077660	(Ne or neon or He or helium or "O.sub.2" or oxygen or Kr or krypton or xe or xenon or "N.sub.2" or nitrogen)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:57
7	BRS	L7	1886	1 same 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:58
8	BRS	L8	281	1 near8 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:58
9	BRS	L9	2235 8556	(@ad<"20020508") or (@rlad<"20020508")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:59
10	BRS	L10	251	8 and 9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 10:59

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	168344	e-beam or "electron beam" or ebeam	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
2	BRS	L2	289365	SiN or "silicon nitride" or Si?N?	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
3	BRS	L3	19113	"self align contact" or SAC or (self-align adj contact)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
4	BRS	L4	455538	cathode or anode	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
5	BRS	L5	55102	(SiH or "NH.sub.3" or "Si.sub.2H.sub.6")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39

	Type	L #	Hits	Search Text	DBs	Time Stamp
6	BRS	L6	3077660	(Ne or neon or He or helium or "O.sub.2" or oxygen or Kr or krypton or xe or xenon or "N.sub.2" or nitrogen)	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
7	BRS	L7	1886	L1 same L2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
8	BRS	L8	281	L1 near8 L2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
9	BRS	L9	2235 8556	(@ad<"20020508") or (@rlad<"20020508")	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
10	BRS	L11	2347	PMOSFET	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:44

	Type	L #	Hits	Search Text	DBs	Time Stamp
11	BRS	L10	251	L8 and L9	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:39
12	BRS	L13	4	10 and MOSFET	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:48
13	IS&R	L14	4	(("5003178") or ("6407399")).PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:55
14	IS&R	L15	0	("10428374").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:55
15	IS&R	L16	0	("10428374").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:57

	Type	L #	Hits	Search Text	DBs	Time Stamp
16	IS&R	L17	2	("20030064607").PN.	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 14:58
17	BRS	L18	3	("2003/0064607").URPN.	USPAT	2004/11/17 15:18
18	BRS	L19	2	("4165517" | "4585489").PN.	US-PGPUB; USPAT; USOCR	2004/11/17 15:19
19	BRS	L20	2	("4165517" | "4585489").PN.	US-PGPUB; USPAT; USOCR	2004/11/17 15:20
20	BRS	L21	3	("5808352").URPN.	USPAT	2004/11/17 15:20
21	BRS	L22	3	("5808352").URPN.	USPAT	2004/11/17 15:21
22	BRS	L23	2	("4165517" | "4585489").PN.	US-PGPUB; USPAT; USOCR	2004/11/17 15:22

	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L2	3	silicon adj nitride same electron adj beam same treating	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 18:49
2	BRS	L3	33	silicon adj nitride same electron adj beam same treated	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	2004/11/17 18:49

DOCUMENT-IDENTIFIER: US 20030134039 A1

TITLE: Electron beam modification of CVD deposited films,
forming low dielectric constant materials

---------- KWIC ---------

Detail Description Paragraph - DETX (10):
[0036] A 4" silicon wafer inserted into a cluster tool having an interconnected chemical vapor deposition module and an **electron beam** exposure module. A vacuum is applied through the entire tool including the **electron beam** exposure module, the chemical vapor deposition module and a transport zone between the modules. The wafer is transported to the chemical vapor deposition module where the surface of the wafer is applied with a layer of **silicon nitride** by chemical vapor deposition. Without breaking the vacuum, the **treated** wafer is transported to the **electron beam** exposure module where it is exposed to **electron beam** radiation using a large area electron source while being heated. The cold-cathode source produces a large area **electron beam** (over 200 mm in diameter) having a substantially uniform emission over its entire surface. Electron emission is controlled by the low bias voltage applied to the anode grid. **Electron beam** exposure was conducted at a temperature of 350.degree. C. and in an argon atmosphere (10-30 milliTorr). The dose is 10,000 .mu.C/cm.sup.2. The **electron beam** current is 30 mA. The energy is 20 keV. After removal from the tool, the **silicon nitride** layer has a dielectric constant of less than 3.

US-PAT-NO: 5808352

DOCUMENT-IDENTIFIER: US 5808352 A

TITLE: Semiconductor apparatus having crystal defects

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Application Filing Date - AD (1):
19960920

Brief Summary Text - BSTX (2):
The present invention relates to semiconductor apparatus such as diodes, transistors, thyristors and MOSFETs and a process for fabricating them. More particularly, the invention relates to semiconductor apparatus that have not only fast switching characteristics but also high breakdown voltage or small leakage current characteristics. The invention also relates to a process for fabricating such semiconductor apparatus.

Brief Summary Text - BSTX (11):
Another problem with this technique is that in the case of a MOSFET, irradiation with particle rays such as electron beams creates positive charges or other minority carriers in the gate insulating film, thereby increasing the gate-to-source leakage current.

Brief Summary Text - BSTX (21):
In another preferred embodiment, said device is a vertical MOSFET comprising a semiconductor layer of a first conduction type, a semiconductor region of a second conduction type that is provided in said semiconductor layer and that has a channel region at either end and a source region provided at either end of said semiconductor region of a second conduction type, said crystal defects being formed both within and below said semiconductor region of a second conduction type in said vertical MOSFET whereas said silicon nitride film is

provided above the gate electrode of said vertical MOSFET. This arrangement is also effective in providing the vertical MOSFET with fast switching characteristics and, at the same time, it is capable of maintaining the gate-to-source leakage current at a reasonably small level.

Detailed Description Text - DETX (7):

To fabricate the transistor of Example 1, the silicon nitride film 17 is provided before the semi-conductor layer 11 is given overall exposure to an electron beam to create crystal defects 21 in that layer 11. Many crystal defects 21 are formed under the base region 12 but only few crystal defects 21 are created in the field region which surrounds the base region 12 (the number of crosses in FIG. 1 is a relative measure of the number of crystal defects present). Thus, the silicon nitride film 17 which restrains the exposure to an electron beam is provided in the surface of the semiconductor layer 11 to cover the field region before actual exposure to electron beams. Because of this configuration, an electron beam is admitted unattenuated into the semiconductor layer 11 in the base region 12 which has no overlying silicon nitride film, thereby creating many crystal defects 21. On the other hand, the field region which is provided with the silicon nitride film 17 effectively restrains the penetration of the electron beam so that only a limited amount of the electron beam will reach the semiconductor layer 11 to create a correspondingly smaller number of crystal defects 21.

Detailed Description Text - DETX (9):

The transistor of Example 1 is fabricated by performing exposure to particle rays such as an electron beam after the provision of the silicon nitride film 17 and, hence, the lifetime of carriers is sufficiently shortened in the dominant current path under the base region 12 to provide fast switching characteristics. On the other hand, the exposure to electron beams

is
restrained in the field region by means of the silicon nitride film 17 and the
creation of crystal defects 21 is suppressed accordingly to ensure against the
drop in dielectric breakdown strength. The crystal defects 21 created upon
irradiation with an electron beam are repaired by annealing at 450.degree. C.
or below, so exposure to an electron beam is preferably performed after the
post-diffusion anneal step which is conducted at elevated temperatures. In
contrast, the silicon nitride film 17 can safely be left intact on the final
product without causing any problems. Therefore, irradiation with an electron
beam may be performed at all times subsequent to annealing. On the other hand,
the silicon nitride film 17 can withstand elevated temperatures and, hence, may
be formed at the early stage of a fabrication process for the transistor; if
desired, the film may also serve as a mask to form the base region 12.

Detailed Description Text - DETX (12):

The concept of the invention for controlling the lifetime of carriers was
applied to a vertical MOSFET. Reference should first be made to FIG. 3. A
semiconductor substrate 30 of a first conduction type, say, n.sup.+ type has
formed thereon an n-type semiconductor layer 31, a semiconductor region 32 of a
second conduction type, say, p-type, with the channel region indicated by 32a,
n.sup.+ type source regions 33, a gate insulator film 34, a gate electrode 35,
a silicon nitride film 36 for restraining the exposure to particle rays such as
electron beams, a source electrode 37 and a drain electrode 38. Crystal
defects 39 which have been created by exposure to particle rays such as
electron beams are designated by the same convention as in FIG. 1. To gain a
large current, the MOSFET shown in FIG. 3 has a matrix of many cells that each
consist of the source regions 33 and the channel region 32a and which

are
formed within the semiconductor layer 31 providing the drain region. A current
flows vertically from the source regions 33 of each cell through the channel
region 32a to the back surface of the semiconductor layer 31 and the sum of
such currents flowing through all cells that are present provides the drain
current of the MOSFET. In a MOSFET of the type under discussion, a pn junction
40 is formed between the p-type region 32 and the n-type semiconductor layer 31
and a diode is established in this region. Loss will occur if this diode,
generally called a "built-in diode" has a long reverse recovery time (trr). In
Example 2, an electron beam is applied to this region to create crystal defects
39, whereby the lifetime of carriers is sufficiently shortened to reduce the
reverse recovery time (trr) of the built-in diode (i.e. enable its quick
reverse recovery).

Detailed Description Text - DETX (15):
FIG. 4 shows the profile of the gate-to-source leakage current I.sub.GSS of
the vertical MOSFET of Example 2, as measured on 20 samples. FIG. 4 also shows
as comparative data the profile of the I.sub.GSS of a vertical MOSFET that had
the switching characteristics improved by the prior art overall exposure to an
electron beam. Obviously, the leakage current flowing through the invention
transistor was about one tenth the value for the prior art product.

Claims Text - CLTX (6):
3. A semiconductor apparatus according to claim 1, wherein said apparatus
is a vertical MOSFET comprising a semiconductor layer of a first conduction
type, a semiconductor region of a second conduction type that is provided in
said semiconductor layer and that has two ends and a channel region at each end
and a source region provided at each end of said semiconductor region of a
second conduction type, said crystal defects being formed both within

and below
said semiconductor region of a second conduction type in said
vertical MOSFET
whereas said silicon nitride film is provided above a gate electrode
of said
vertical MOSFET.